REMARKS

I. Response to Restriction Requirement

In response to Examiner's Election/Restriction requirement under 35 U.S.C. 121, Applicants elect to pursue initially prosecution of what the Examiner refers to as "Invention I" (*i.e.*, claims 1-22). This election is made without traverse.

II. Status of the Claims

Claims 1-62 are pending in this application. Claims 1-22 have been rejected, and the Examiner has withdrawn from consideration claims 23-38 "as being drawn to an non-elected invention." Claims 39-62 are added herein.

III. Rejections Under 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 6-9, 11-14, and 18-21 "under 35 U.S.C. 102(b) as being anticipated by Shin et al. (US 6,395,578 B1)." *See* Office action at pages 3-6. Applicants respectfully traverse these rejections.

Claim 3 has been amended to recite explicitly the limitations of independent base claim 1. Claim 3 recites a method including, among other things, (1) applying a strip to a second surface of a substrate, (2) removing the strip from the substrate, and (3) attaching a thermal element to an exposed surface of a semiconductor die.

The Examiner has argued at pages 4-5 of the Office action that the Shin *et al.* reference discloses a fabrication method that includes "applying a closure member (70) (a strip) to said second surface of said substrate," "removing said a closure member (70) (a strip) from said substrate (11)(see Figure 7A-7E)," and also "attaching a thermal element to said exposed surface of said semiconductor die (see Figure 7E)." Applicants respectfully disagree.

In particular, Applicants note that the Shin *et al.* reference does not disclose or suggest ***both*** "applying a closure member (70) (a strip) to said second surface of said substrate," and also "attaching a thermal element to said exposed surface of said semiconductor die (see Figure 7E)," as the Examiner has argued. Applicants submit that Figure 7E of the Shin *et al.* reference at best may only disclose removal of the closure member (70). But this figure (and indeed the Shin *et al.* reference as a whole) does not also disclose or suggest both "applying a closure member (70)" and "attaching a thermal element." For at least this reason, Applicants respectfully submit that claim 3 is not anticipated by the Shin *et al.* reference.

Claim 1 has been cancelled. Claims 2, 6-9, 11-14, and 18 depend on claim 3, and thus also are not anticipated by Shin *et al.*

Amended claim 19 recites a method including, among other things, (1) applying a strip to a second surface of a substrate, (2) removing the strip from the substrate, and (3) attaching a thermal element to the exposed surface of each semiconductor die. As discussed above with reference to claim 3, Applicants respectfully submit that the Shin *et al.* reference does not disclose or suggest both "applying a closure member" to a second surface of a substrate as well as "attaching a thermal element" to the exposed surface of each semiconductor die as the Examiner has argued. For at least this reason, Applicants respectfully submit that amended claim 19 is not anticipated by the Shin *et al.* reference.

Claims 20-21 depend, directly or indirectly, on claim 19, and thus are also not anticipated Shin *et al.*

In addition, Applicants respectfully note that the Shin *et al.* reference ***explicitly teaches away*** from an assembly method that includes the attachment of a heat discharge plate or

heat sink. In particular, the "Background of the Invention" section of the Shin *et al.* reference states:

> Although a semiconductor package has been proposed, which is provided with a heat discharge plate or heat sink for easily discharging heat generated from the semiconductor chip, ***the provision of such a heat discharge plate causes another problem because it serves to further increase the thickness of the semiconductor package while increasing the manufacturing costs.***

See Shin *et al.* at column 2, lines 18-24 (emphasis added by Applicants). The Shin *et al.* reference therefore provides at least two reasons—increased package thickness and increased manufacturing costs—why it is undesirable to employ an assembly method that includes the attachment of a heat discharge plate or a heat sink to a semiconductor chip.

As even further teaching away from the methods recited in claims 3 and 19, the Shin *et al.* reference teaches that a copper layer closure member (70) may remain attached—and never be removed—"to improve the heat discharge performance of the semiconductor chip 30." *See* Shin *et al.* at column 7, lines 43-46; *see also* column 9, lines 32-36 ("For the closure members 70, copper layers exhibiting a superior heat discharge property also may be attached to the circuit board strip 10. In such a case, the closure members 70 are ***not removed*** after the completion of the package fabrication.") (emphasis added by Applicants) and column 10, lines 30-33 ("It is also possible to deliver the semiconductor packages in a state in which the closure members 70 are ***not removed***, for example, where the closure member is made of a copper layer.") (emphasis added by Applicants).

For at least these reasons, Applicants submit that claims 2-3, 6-9, 11-14, and 18-21 are not anticipated by U.S. Patent No. 6,395,578 B1. Applicants thus respectfully request that

the rejections of claims 2-3, 6-9, 11-14, and 18-21 under 35 U.S.C. § 102 be withdrawn, and that the pending claims be allowed.

IV. Rejections Under 35 U.S.C. § 103(a)

A. Shin *et al.* In View of Juskey *et al.*

The Examiner has rejected claims 4-5, 15-17, and 22 "under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. 6,395,578 B1) in view of Juskey et al. (U.S. 6,507,102 B2)." *See* Office action at pages 3 and 7. Applicants respectfully traverse these rejections.

Claims 4-5 and 15-17 depend, directly or indirectly, on claim 3. As mentioned above, the Shin *et al.* reference fails to disclose or suggest a method that includes both "applying a closure member (70) (a strip) to said second surface of said substrate," "removing said a closure member (70) (a strip) from said substrate (11)" as well as "attaching a thermal element to said exposed surface of said semiconductor die" as the Examiner has argued. The Examiner has not argued that the Juskey *et al.* reference provides such a disclosure or suggestion. Thus, even assuming *arguendo* that it is proper to combine the teachings of the Shin *et al.* and Juskey *et al.* references as the Examiner has suggested (which Applicants do not concede is a proper combination), such a combination would not achieve the method recited in claim 3.

Claim 22 depends indirectly on claim 19. For the reasons discussed above, Applicants respectfully submit that the Examiner has not shown that amended claim 19 is disclosed or taught by either the Shin *et al.* reference alone, or by a combination of the Shin *et al.* reference with the Juskey *et al.* reference.

Applicants therefore respectfully request that the rejection of claims 4-5, 15-17, and 22 under § 103(a) be withdrawn, and that the pending claims be allowed.

B. Shin *et al.* In View of Combs

The Examiner has rejected claim 10 "under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. 6,395,578 B1) in view of Combs (U.S. 5,596,231)." *See* Office action at pages 3 and 7-8. Applicants respectfully traverse this rejection.

Claim 10 depends indirectly on claim 3. As mentioned above, the Shin *et al.* reference fails to disclose or suggest a method that includes both "applying a closure member (70) (a strip) to said second surface of said substrate" as well as "attaching a thermal element to said exposed surface of said semiconductor die" as the Examiner has argued. The Examiner has not argued that the Combs reference provides such a disclosure or suggestion. Rather, the Examiner's reference to Combs is limited to the statement that "Combs discloses a semiconductor package with (10) said interconnecting comprising a thereto-sonic [sic] wire bonding process (see column 6, lines 53-60)." *See* Office action at page 8. Thus, even assuming *arguendo* that it is proper to combine the teachings of the Shin *et al.* and Combs references as the Examiner has suggested (which Applicants do not concede is a proper combination), such a combination would not achieve the method recited in claim 3.

Applicants therefore respectfully request that the rejection of claim 10 under § 103(a) be withdrawn, and that the pending claim be allowed.

V. Form PTO 1449

Applicants respectfully request confirmation that the Examiner has reviewed and considered both the Amkor Technology Data Sheet and the U.S. Non-Provisional Patent Application listed on the Form PTO-1449 submitted with Applicants' January 28, 2003 Information Disclosure Statement. For the Examiner's convenience, a new Form PTO-1449 including only these two items has been submitted herewith.

In addition, Applicants ask the Examiner to confirm that he has reviewed the materials submitted with the April 15, 2003 and April 30, 2003 Information Disclosure Statements. For the Examiner's convenience, Applicants have also submitted herewith copies of the Form PTO-1449 papers provided on April 15 and April 30, 2003.

VI. Conclusion and Request for Reconsideration

Applicants request reconsideration of the present application in view of the aforementioned amendments and remarks. Although other features of the claims in the present application are also significant, Applicants respectfully submit that the pending claims are allowable for at least the aforementioned reasons. Accordingly, Applicants respectfully request that the rejections under §§ 102(b) and 103(a) be withdrawn, and that the pending claims be allowed.

In the event that a telephone conference would advance examination of this application, the Examiner is invited to contact the undersigned at the number provided.

VII. Authorization

Applicants have submitted herewith a Petition for Extension of Time, which requests a one month extension of time for filing this Amendment. In the event that the Commissioner determines that an additional extension of time or additional fees are due for this paper, the undersigned hereby petitions for any required extension of time, and authorizes the

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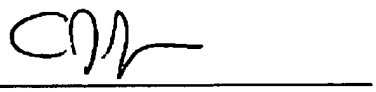
Commissioner to charge any fee required to Milbank's deposit account no. 13-3250, order no. 36080-01101. A DUPLICATE COPY OF THIS PAGE IS ENCLOSED HEREWITH.

Respectfully submitted,
Milbank, Tweed, Hadley & McCloy LLP



Christopher J. Gaspar
Reg. No. 41,030

November 20, 2003

Milbank Tweed Hadley & McCloy LLP
1 Chase Manhattan Plaza
New York, NY 10005
(212) 530-5000 / (212) 530-5219 (facsimile)

NY2:#4515636

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 36080.01101	SERIAL NO. 10/062,650
INFORMATION DISCLOSURE CITATION	APPLICANT Neil R. McLellan	
(Use several sheets if necessary)	FILING DATE January 31, 2002	GROUP ART UNIT 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,172,213	12/15/92	Zimmerman			
		5,485,037	1/16/96	Marrs			
		5,854,511	12/29/98	Shin et al.			
		6,091,603	7/18/00	Daves et al.			
		6,104,086	8/15/00	Ichikawa et al.			
		6,236,568	5/22/01	Lai et al.			
		6,265,771	7/24/01	Ference et al.			
		2002/0079570	6/27/02	Ho et al.			

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,693,572	12/2/97	Bond et al.			
		5,679,978	10/21/97	Kawahara et al.			
		6,396,143	5/28/02	Kimbara et al.			
		5,620,928	4/15/97	Lee et al.			
		6,433,360	8/31/02	Dosdos et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,498,099	12/24/02	McLellan et al.			
		2001/0000924A1	5/10/01	Karnezos et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)

			Amkor Technology, www.amkor.com, Data Sheet for Laminate, Rev. Date 1/01 (2pages)
			U.S. Non-Provisional Patent Application for "Enhanced Thermal Dissipation Integrated Circuit Package and Method of Manufacturing Enhanced Thermal Dissipation Integrated Circuit Package" (Serial No. 09/902,878)

EXAMINER	DATE CONSIDERED

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